REMARKS

Claims 1, 2 and 13 have been amended, and new claims 15-20 have been added. Claim 1 has been amended to clarify its intent and to further define the invention. Claim 2 was amended to correct an informality. The new claims are directed to preferred embodiments that are disclosed in the specification and other claims. Thus, claims 1-20 appear in this application for the Examiner's review and consideration.

The Examiner noted an informality in claim 2, and that claim has been amended as suggested to correct the informality. In particular, claim 2 now recites "annealing the wafer by heating" which is a cosmetic change. No new matter has been added by any of the claim changes or additions, so that these changes should be entered at this time.

Claims 1, 10 and 13 were rejected as being anticipated by Imaoka et al. U.S. patent 5,426,073.

Imaoka discloses a method for fabricating semiconductor devices that includes using an intermediate grinding step. Figs. 3(a) to 3(c) illustrate fabrication steps of a preferred embodiment, wherein a silicon semiconductor wafer 1 has multiple layers 2 formed thereon, a grinding step is utilized, and then a passivation film 4 is formed (see Imaoka, col. 4, lines 21-32). The passivation layer 4 is deposited to cover the entire wafer, and comprises a PSG film 4-1 and silicon nitride film 4-2 for passivating the IC elements. The passivation layer is provided to finish the wafer process (see col. 5, lines 52-57). Figs. 7(a) to 7(c) of Imaoka illustrate a second embodiment wherein an etching process is used instead of a grinding process on a multiple layer 2 to remove an abnormal protrusion. Similar to the method of the first embodiment, element isolating regions are fabricated as shown in Fig. 7(a), a protection layer of photo-resist is deposited, and then each of the multiple layers is etched away until an uncovered peripheral portion 1' of the underlying silicon substrate is exposed (see Fig. 7(b)). The protection layer is then removed, a wire pattern is formed and finally a passivation layer 4 is deposited to cover the entire wafer and to end the wafer process (see Fig. 7(c) and col. 7, line 44 to col. 8, line 13).

In contrast, the present invention is a treatment that utilizes a pre-existing useful layer to encapsulate an exposed edge of an intermediate layer of a multilayer semiconductor structure. In particular, independent claims 1 and 13 recite that the method includes treating the wafer to cause a portion of the surface layer to encapsulate the exposed lateral edge of the intermediate layer to prevent attack on the peripheral edge during subsequent treatments of the wafer. Claim 13 has been amended to recite that the surface layer is monocrystalline, to

make it clear that a single encapsulating material is used. Conversely, Imaoka discloses depositing a passivation layer which includes multiple material layers (PSG and silicon nitride layers). Yet further, Imaoka teaches to cover the entire wafer, and that encapsulating the IC elements that have been fabricated finishes the wafer process. Such procedures are different from that of the present claims. The applicants therefore respectfully assert that Imaoka fails to suggest or teach a method that utilizes the monocrystalline material of the surface layer to encapsulate the edge portion of the intermediate layer, and thus claims 1 and 13 are not anticipated. In addition, the applicants assert that claims 1 and 13 are patentably distinct from Imaoka. Since claim 10 depends on claim 1, it should be allowable for at least the same reasons.

Claims 1, 2, 6 and 10-14 were rejected for allegedly being anticipated by Iwamatsu et al., U.S. patent 6,150,696.

Iwamatsu pertains to a semiconductor substrate and method of fabricating a semiconductor device which prevents particles of dust from being produced at an edge of the substrate. In order to accomplish this goal, Iwamatsu teaches to form a first oxide film to cover a central section and the edge section of the substrate, to then selectively form an oxidation-resistant film on the first oxide film in the central section, to further oxidize the edge section using the oxidation-resistant film as a mask to form a second oxide film in the edge section, and to then form semiconductor elements in the active region (see Iwamatsu patent, col. 2, line 58 to col. 3, line 7). Iwamatsu thus teaches to thin the SOI layer 3 by further oxidizing the oxide film 21 to form the second oxide film 23, which results in reducing the silicon islands SI in the edge section of the SOI substrate (see Figs. 8-10 and col. 11, lines 2-21). In another aspect, Iwamatsu discloses a method for protecting the lateral edge section by using an oxide film 31 and a nitride film 32 to entirely cover the SOI substrate (see Figs. 15 to 17, and col. 12, lines 45-57). A second oxide film 33 can also be formed that covers the edge section and the lower major surface of the substrate (see Fig. 18 and col. 13, lines 6-33).

In contrast, as explained above, the present invention is a treatment that utilizes a pre-existing useful layer to encapsulate an exposed edge of an intermediate layer of a multilayer semiconductor structure. The method includes treating the wafer to cause a portion of the surface layer to encapsulate the exposed lateral edge of the intermediate layer to prevent attack on the peripheral edge during subsequent treatments. As also explained above, claim 13 now recites that the surface layer is monocrystalline, and thus the encapsulating portion is

monocrystalline. This is in contrast to the disclosure of Iwamatsu, wherein an oxide film and a nitride film entirely cover the SOI substrate. The applicants therefore respectfully assert that independent claims 1 and 13 are not anticipated, and that these claims are patentably distinct over Iwamatsu. Since claims 2, 6, 10 and 14 all depend on either claim 1 or claim 13, these claims should be allowable for at least the same reasons.

In view of the above amendments and remarks, the applicants respectfully request withdrawal of all of the 35 U.S.C. 102(b) rejections of the claims.

Claims 7-9 were rejected at being unpatentable over Iwamatsu and Applicants' Admitted Prior Art ("AAPA") found on pages 1-2 of the application.

For the reasons explained above, independent claim 1 is patentably distinct from Iwamatsu. Since claims 7-10 all directly or indirectly depend on claim 1, they should be allowable for at least the same reasons. The alleged admissions made by the applicants do not remedy the deficiencies of the Iwamatsu patent. Thus, the applicants respectfully request withdrawal of the 35 U.S.C. 103(b) rejections of claims 7-10.

It is noted that claims 3-5 were objected to as being dependent on a rejected base claim, but would be allowable if rewritten. The applicants have thus added new claim 16 which includes the elements of original claims 1, 2 and 3, as suggested. Thus, claim 16 is believed to be patentably distinct over the cited art, and dependent claims 17-20 should be allowable for at least the same reasons.

In view of the above, the entire application is believed to be in condition for allowance, early notice of which would be appreciated. Should any issues remain, a personal or telephonic interview is respectfully requested to discuss the same in order to expedite the allowance of all the claims in this application.

Respectfully submitted,

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